REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-30 are pending. Claims 1, 5, and 7-10 have been amended. Claim 4 has been cancelled without prejudice. No claims have been added. Therefore, claims 1-3 and 5-30 are now presented for examination.

Provisional Double Patenting Rejection

The Examiner has provisionally rejected the claims based on the judicially created doctrine of double patenting based on co-pending U.S. application No. 09/967,220.

On behalf of the applicant, it is submitted that the co-pending application is commonly owned with the current application. A terminal disclaimer of the terminal portion of patents resulting from co-pending U.S. application No. 09/967,220 has been executed by a registered attorney of record and is filed concurrently herewith.

Claim Objections

The Examiner has objected to claims 7-9 because of informalities. The claims have corrected to refer consistently to an event monitoring "component", rather than an event monitoring "apparatus".

Claim Rejection under 35 U.S.C. §102

Levine, et al.

The Examiner rejected claims 1, 2, 4-17, 21, 22, and 24-30 under 35 U.S.C. 102 (e) as being anticipated by U.S Patent 6,134,710 of Levine, et al. ("Levine").

As amended here, claim 1 provides as following:

1. An event monitoring component for dynamic optimization comprising:

an event monitor to selectively capture a plurality of profiles of one or more microarchitecture events occurring in the execution of an application by a microprocessor based upon configuration information supplied by a software component;

a profile buffer to store the plurality of captured profiles of the one or more microarchitecture events; and

an interface through which the software component provides the configuration information to direct the operation of the event monitor.

Thus, claim 1 provides for a event monitor that captures a plurality of profiles of microarchitecture events, and for a profile buffer to store the captured profiles. It is submitted that, if Levine is examined closely, it is clear that Levine describes a different type of operation.

In Figure 7 of Levine, the operation of the Levine process is illustrated. One of the performance monitor counters is shown as element 130. Also shown is an interrupt 570, with a sampled instruction address register (SIAR) 530 and a sampled data address register (SDAR) 540. As described in Levine, the operation of the system is such that the counter 130 counts the number of times that a particular event occurs. When the counter reaches a certain number, an interrupt 570 is triggered. As indicated in Levine, "[w]hen enabled, interrupts are generated when the most significant bit of the selected counter transitions from a logical 0 to a logical 1. Typically, when an interrupt is generated, the state of processor registers is saved as well as the effective address of the executing instruction. Upon an interrupt, the effective address of the executing instruction and the

executing instruction operand are saved in the sampled instruction address register, SIAR, and the sampled data address register, SDAR, respectively. The state of the execution units is also saved on interrupt." (Levine, col. 8, lines 25-35)

Levine thus describes a system in which counters are utilized to count certain events. When a counter reaches a certain point, an interrupt is triggered to hold information. In short, the Levine system generally is just counting, and only collects information when an interrupt status is reached.

In contrast, claim 1, as amended, provides that profiles of one or more microarchitecture events are captured and stored, which is a different and more intensive operation than that described in Levine. Rather than simply counting events, claim 1 provides that profiles of events are captured and stored in a profile buffer. In Levine, address information is obtained only when a counter reaches a certain level and an interrupt occurs. Therefore Levine describes a lower level process that is intended to count the number of times that one or more different events occur, and then interrupt the process when a sufficient number of events reached. When an interrupt is triggered, the appropriate address information for the instruction and connected data are saved.

To explain the differences further, when an interrupt occurs in Levine, all that will have been saved at that time is the address information and current data regarding a particular event. In contrast, claim 1 provides for collecting a plurality of profiles of events, thereby providing greater event data. As is clear from the description, Levine is intended to solve a narrow type of problem, which is to address long table walks and cache misses. The solution proposed by Levine is limited to a structure that will allow for detection of this problem and the addition of a preload instruction prior to the address

of an instruction that creates the problem. As such, Levine does not teach or suggest the collection of multiple event profiles.

It is submitted that the above arguments are also applicable to independent claims 10 and 21, and for at least these reasons the claims are patentable. The remaining rejected claims are dependent claims and, in addition to other reasons, are allowable as being dependent on the allowable base claims.

Claim Rejection under 35 U.S.C. §103

Levine, et al.

The Examiner rejected claims 3, 18-20, and 23 under 35 U.S.C. 103 (a) as being unpatentable over Levine as applied to claim 2, 10, and 22, respectively.

In addition to other reasons, it is submitted that the claims are dependent on allowable base claims, as shown above, and thus the claims are not unpatentable over Levine.

Amendments to the Specification

The specification has been amended to correct minor typographical errors in paragraphs [0032] and [0046].

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (503) 439-8778 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for a one-month extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a). A check is enclosed to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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Date: 12/15/04

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